## REMARKS

Reconsideration of the above-referenced application in view of the above amendment, and of the following remarks, is respectfully requested.

Claims 1-10 and 21-25 are pending in this case. Claims 11-20 are canceled herein. Claims 21-25 are added herein to more completely cover that which Applicant regards as the invention.

The Examiner rejected claims 1-3, and 5 under 35 U.S.C. § 102(e) as being anticipated by Oda (U.S. 6,316,833).

Applicant respectfully submits that claim 1 is unanticipated by Oda as there is no disclosure or suggestion in Oda of a porous dielectric material doped with at least one dopant located between the semiconductor device and a contact layer operable to provide electrical connection to the semiconductor device. Oda teaches a porous dielectric layer doped with fluorine. However, the porous dielectric layer 10 is used above the first metal interconnect layer 7, not inwardly of the first metal interconnect layer 7. The dielectric layer 4 of Oda is located inwardly of the first metal interconnect layer 7. Dielectric layer 4 is not taught as being porous. While the porous dielectric layer 10 of Oda is located inwardly of the second metal interconnect layer 16, interconnect layer 16 is not operable to provide electrical connection to the semiconductor device as required by the claim. Accordingly, Applicant respectfully submits that claim 1 and the claims dependent thereon are unanticipated by Oda.

The Examiner rejected claims 4 and 6-10 under 35 U.S.C. § 103(a) as being unpatentable over Oda (U.S. 6,316,833) in view of Tseng (U.S. 5,728,618).

Applicant respectfully submits that claim 4 is patentable over Oda in view of Tseng for the same reasons discussed above relative to claim 1 from which claim 4 depends. Tseng is added to teach a FET as a semiconductor device structure.

Applicant respectfully submits that claim 6 is patentable over the references as there is no disclosure or suggestion in the references of porous dielectric material doped with at least one dopant located between the semiconductor substrate and a contact layer operable to provide electrical connection to the source and drain regions. Oda teaches a porous dielectric layer doped with fluorine. However, the porous dielectric layer 10 is used above the first metal interconnect layer 7, not inwardly of the first metal interconnect layer 7. The dielectric layer 4 of Oda is located inwardly of the first metal interconnect layer 7. Dielectric layer 4 is not taught as being porous. While the porous dielectric layer 10 of Oda is located inwardly of the second metal interconnect layer 16, interconnect layer 16 is not operable to provide electrical connection to the source and drain regions as required by the claim. Accordingly, Applicant respectfully submits that claim 6 and the claims dependent thereon are patentable over the references.

Applicant respectfully submits that newly added claim 21 is patentable over the references as there is no disclosure or suggestion of a pre-metal dielectric layer between the lowermost metal interconnect layer and the semiconductor substrate, the pre-metal dielectric comprising an at least substantially porous dielectric material doped with at least one dopant. As discussed above, Oda only teaches using its porous dielectric above the first metal interconnect layer. Oda does not disclose or suggest using the porous dielectric as a pre-metal dielectric below the lowermost metal interconnect layer. Accordingly, Applicant respectfully submits that claim 21 and the claims depend nt th reon are patentable over the references.

In light of the above, Applicant respectfully requests withdrawal of the Examiner's rejections and allowance of claims 1-10 and 21-25. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

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